

Form 1449*	Atty. Docket No.: 303.523US2	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Leonard Forbes et al.	
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U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>DHL</i>	3,582,915	06/01/1971	Chow, W.F.	340	174	10/16/69
<i>DHL</i>	4,051,354	09/27/1977	Choate, W.C.	235	312	07/03/75
<i>DHL</i>	4,528,583	07/09/1985	te Velde, T.S., et al.	357	71	04/19/84
<i>DHL</i>	4,635,091	01/06/1987	Roger, B.P.	357	67	08/10/84
<i>DHL</i>	4,968,643	11/06/1990	Mukai, R.	437	174	04/26/89
<i>DHL</i>	5,256,899	10/26/1993	Rangappan, A.	257	665	12/24/91
<i>DHL</i>	5,303,199	04/12/1994	Ishihara, H., et al.	365	225.7	02/19/91
<i>DHL</i>	5,327,380	07/05/1994	Kersh, III, D.V., et al.	365	195	02/08/91
<i>DHL</i>	5,604,693	02/18/1997	Merritt, T.A., et al.	365	96	08/16/95
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<i>DHL</i>	5,936,297	08/10/1999	Jun, Y.K.	257	530	03/24/97
<i>DHL</i>	6,080,649	06/27/2000	Werner, W., et al.	438	601	01/08/97

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
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<i>DHL</i>	Baek, J.T., et al., "A new low-resistance antifuse with planar metal/dielectric/poly-Si/dielectric/metal structure", <u>Abstract, Japanese Journal of Applied Physics, Part 1, 36 (3B) (Regular Papers, Short Notes & Review Papers)</u> , Abstract No. B9707-2530F-004, (March 1997)
<i>DHL</i>	Fujishiro, F., et al., "Effects of resist strip processing damage on the electrical characteristics of 0.8-micron a-Si antifuse circuit elements", <u>Abstract, Proceedings of the SPIE - The International Society for Optical Engineering, 2334</u> , Austin, TX, Abstract No. B9504-1265-011, (Oct. 20-21, 1994)
<i>DHL</i>	Gordon, K.E., et al., "Conducting filament of the programmed metal electrode amorphous silicon antifuse", <u>Abstract, Proceedings of the IEEE International Electron Devices Meeting, Technical Digest</u> , Washington, D.C., Abstract No. B9412-1265D-014, (Dec. 5-8, 1993)
<i>DHL</i>	Hamdy, E., et al., "Dielectric based antifuse for logic and memory ICs", <u>IEDM</u> , San Francisco, Ca, pp. 786-789, (1988)
<i>DHL</i>	Hodges, D.A., et al., "MOS Decoders", <u>In: Analysis and Design of Digital Integrated Circuits, 2nd Edition</u> , Section: 9.1.3, 354-357, (1988)

Examiner <i>Kang, Donghee</i>	Date Considered <i>3-6</i>
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*Substitute Disclosure Statement Form (PTO-1449)

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<i>nm</i>	Shih, C., et al., "Characterization and modeling of a highly reliable metal-to-metal antifuse for high-performance and high-density field-programmable gate arrays", <u>Abstract, Proceedings of the 35th Annual IEEE International Reliability Physics Symposium</u> , Denver, CO, Abstract No. B9709-2570D-023, (April 8-10, 1997)
<i>nm</i>	Zhang, G., et al., "Reliable metal-to-metal oxide antifuses", <u>Abstract, Proceedings of the IEEE International Electron Devices Meeting, Technical Digest</u> , San Francisco, CA, Abstract No. B9504-2530G-001, (Dec. 11-14, 1994)

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